AMENDMENTS TO THE SPECIFICATION:

Page 10, please further amend the paragraph beginning on line 14 and bridging pages 10 and 11 as follows:

--According to the fourth aspect of the present invention, there is provided a program ~~embodied in a computer-readable medium~~ for allowing a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O cell on a chip, which are to be connected to external pins, to execute a first process of computing a wiring length of a sub net between adjoining I/O cells for test signals (called "test net") to be wired to an area for layout of I/O cells (called "I/O area") at a peripheral portion of a chip by referring to the I/O cell layout position information, I/O cell size information and I/O cell test terminal information in the memory unit and outputting the wiring length; a second process of computing information at least on a wiring resistance and a capacitance for the sub net, causing a circuit simulator to execute circuit simulation to acquire a wiring delay of the sub net and waveform depression at an end of the sub net; a third process of determining an optimal repeater circuit to be inserted in an empty cell where the sub net passes, based on the information on the repeater circuit stored in the memory unit in case where the

wiring delay and waveform depression concerning the sub net are out of a predetermined range of allowance defined in the technology information; and a fourth process of laying out an empty cell including the determined repeater circuit in the I/O area.--